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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/556,472	04/21/2000	Michael Andrew Mang	0100.0000600	6793

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EXAMINER
MONESTIME, MACKLY

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/556,472	Mang et al
Examiner	**Group Art Unit**
Mackey Monestime	2676

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☑ Responsive to communication(s) filed on 4/21/00.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) 1-14 is/are pending in the application.

Of the above claim(s) ____ is/are withdrawn from consideration.

☑ Claim(s) 1-11 is/are allowed.

☑ Claim(s) 12-13 is/are rejected.

☑ Claim(s) 14 is/are objected to.

☐ Claim(s) ____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on ____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on ____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) ____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: ____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). ____

☑ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other ____

Office Action Summary

DETAILED ACTION

1. Claims 1-14 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahsan (US Patent No. 5,119,324) Kanekura (US Patent No. 6,298,364)

4. As per claims 12-13 , Ahsan substantially disclosed the invention as claimed, including a method for executing operation codes in a computational block (col. 1, lines 10-12) comprising: receiving a set of operands during a first cycle (col. 21, lines 17-18), combining the first set of operands using a first operation unit during the first cycle to produce a first result (col. 22, lines 21-25), storing the first operation result in a pre-accumulation buffer during a second cycle to produce a buffered first operation result ; receiving a second set of operands during the second cycle (col. 21, lines 19-20, 25-26) , combining the second set of operands using the first operation unit during the second cycle to produce a second operation result (col. 22, lines 25-30).

Ahsan did not explicitly disclose that selecting a first operand of a third set of potential operands that includes the buffered first operation result, wherein selecting the first operand of the third set of operands occurs during a third cycle, wherein selecting the first operand of the third set of operands is based on a current operation code; and combining the second result and the buffered first operation result using a second operation unit during the third cycle to produce a third operation result. However, Ahsan disclosed that the selected inputs are under control of common signals controlling passing of the instruction from stage to stage in the pipeline (col. 16, lines 62-67; col. 17, lines 1-2). Moreover, the concepts and associated advantages of using a selector or selection means or unit are well known in the art. It can be evidence in the reference by Kanekura in which a selection means coupled to an arithmetic operation for selecting one of the plurality outputs on which the operation resultant data is provided in accordance with a section signal (Fig. 2, Item No. 3; col. 4, lines 65-67; col. 5, lines 19-21). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Kanekura with the teachings of Ahsan because doing so would not only provide a computational block that can carry out a combined operation at high speed and high precision, but also would enhance flexibility by allowing the system to select a single input from a plurality of inputs.

Allowable Subject Matter

5. Claims 1-11 are allowable over the prior art of record.

6. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record failed to teach or disclose either singularly or in combination a method for executing operation code comprising: "wherein storing the first operation result further comprises storing the first operation result in a pre-accumulation buffer of a plurality of pre-accumulation buffers, wherein the pre-accumulation buffer is selected based on a thread of a plurality of threads to which the current operation code corresponds, wherein the set of potential operands includes previously buffered results stored in each of the plurality of pre-accumulation buffers. These distinct features of the present claims invention were not found to be anticipated, suggested or made obvious by the prior art of record.

The prior art of record further failed to teach or disclose either singularly or in combination a circuit comprising: a first and a second operation unit, a pre-accumulation register coupled to the first operation unit and a memory coupled to the second operation unit. Each independent claim identifies the uniquely distinct features: " a selection block coupled to the memory, the second operation unit, the pre-accumulation and the first operation unit, wherein the selection block selects a second operand of the third set of operands from a set of potential operands, wherein the set of potential operands includes the second operation result, the buffered first operation result stored in the pre-accumulation register, and data stored in at least one of the plurality of memory locations of the memory, and wherein the selection block selects the second

operand of the third set of operands based on operand selection information included in an operational code received by the circuit" (as per claims 1 and 6). These distinct features of the present claims invention were not found to be anticipated, suggested or made obvious by the prior art of record.

Conclusion

The prior arts made of record and not relied upon is considered pertinent to applicant's disclosure.

Gahang (US Patent No. 5,838,463) taught a binary image processor.

Beacom et al (US Patent No. 4,996,660) taught a selection of divisor multipliers in a floating point divide circuit.

Oberman et al (US Patent No. 6,085,213) taught a method and apparatus for simultaneously multiplying two or more independent pairs of operands and summing the product.

Sarmiento et al disclosed a High Speed Primitives of Hardware Accelerators DSP In GaAs Technology (IEEE Proceedings-G, Vol. 139, No. 2, April 1992).

Mauro Olivieri disclosed a Design of Synchronous and Asynchronous variable -Latency Pipelined multipliers (IEEE transactions on Very Large Scale Integration Vol. 9 No. 2, April 1992).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mackly Monestime whose telephone number is (703) 305-3855. The examiner can normally be reached on Monday to Thursday from 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bella Matthew, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, Va, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Mackly Monestime
Patent Examiner
October 22, 2002

Matthew C. Bella
Primary Examiner